WHAT IS CLAIMED IS:

1. A driving method of a nonvolatile memory,

wherein during a verify operation, a first operation for changing a threshold voltage of the memory element is performed concurrently with a second operation for judging the threshold voltage of the memory element.

2. A driving method of a nonvolatile memory,

wherein during a verify operation, a first operation for changing a threshold voltage of the memory element by one of charge injection and charge discharge using a tunnel current is performed concurrently with a second operation for judging the threshold voltage of the memory element.

3. A driving method of a nonvolatile memory according to claim 2, wherein a potential difference exists between a source and a drain of the memory element during the second operation.

4. A driving method of a nonvolatile memory,

wherein during a verify operation, a first operation for changing a threshold voltage of the memory element by charge injection using a hot electron is performed concurrently with a second operation for judging the threshold voltage of the memory element.

5. A driving method of a nonvolatile memory according to claim 1,

wherein the first operation and the second operation are terminated and the verify operation is finished at a timing when the threshold voltage of the memory element judged by the second operation becomes a set voltage.

6. A driving method of a nonvolatile memory according to claim 2,

wherein the first operation and the second operation are terminated and the verify operation is finished at a timing when the threshold voltage of the memory element judged by the second operation becomes a set voltage.

7. A driving method of a nonvolatile memory according to claim 4,

wherein the first operation and the second operation are terminated and the verify operation is finished at a timing when the threshold voltage of the memory element judged by the second operation becomes a set voltage.

8. A driving method of a nonvolatile memory for setting a threshold voltage of the memory element at a set voltage or higher,

wherein during a verify operation, a first operation for increasing the threshold voltage of the memory element is performed concurrently with a second operation for judging a relation between the threshold voltage of the memory element and the set voltage,

wherein a result of the second operation is outputted as a verify signal,

wherein the verify signal takes a first value if the threshold voltage of the memory element is smaller than the set voltage, and takes a second value if the threshold voltage of the memory element is larger than the set voltage,

wherein the first operation is performed if the verify signal takes the first value, and is not performed if the verify signal takes the second value, and

wherein the first operation and the second operation are terminated and the verify operation is finished when the verify signal changes from the first value to the second value.

9. A driving method of a nonvolatile memory driving for setting a threshold voltage of the memory element at a set voltage or lower,

wherein during a verify operation, a first operation for decreasing the threshold voltage of the memory element is performed concurrently with a second operation for judging a relation between the threshold voltage of the memory element and the set voltage,

wherein a result of the second operation is outputted as a verify signal,

wherein the verify signal takes a first value if the threshold voltage of the memory element is larger than the set voltage, and takes a second value if the threshold voltage of the memory element is smaller than the set voltage,

wherein the first operation is performed if the verify signal takes the first value, and is not performed if the verify signal takes the second value, and

wherein the first operation and the second operation are terminated and the verify operation is finished when the verify signal changes from the first value to the second value.

10. A driving method of a nonvolatile memory for setting a threshold voltage of a memory element at a set voltage or higher,

wherein during a verify operation, a first operation for increasing the threshold voltage of the memory element is performed concurrently with a second operation for judging a relation between the threshold voltage of the memory element and the set voltage,

wherein the verify operation includes at least a first period and a second period,

wherein a verify signal takes a first value during the first period,

wherein a result of the second operation is outputted as the verify signal during the second period,

wherein during the second period, the verify signal takes the first value if the threshold voltage of the memory element is smaller than the set voltage, and takes a second value if the threshold voltage of the memory element is larger than the set voltage,

wherein the first operation is performed if the verify signal takes the first value, and is not performed if the verify signal takes the second value, and

wherein the first operation and the second operation are terminated and the verify operation is finished when the verify signal changes from the first value to the second value.

11. A driving method of a nonvolatile memory for setting a threshold voltage of a memory element at a set voltage or lower,

wherein during a verify operation, a first operation for decreasing the threshold voltage of the memory element is performed concurrently with a second operation for judging a relation between the threshold voltage of the memory element and the set voltage,

wherein the verify operation includes at least a first period and a second period,

wherein a verify signal takes a first value during the first period,

wherein a result of the second operation is outputted as the verify signal during the second period,

wherein during the second period, the verify signal takes the first value if the threshold voltage of the memory element is larger than the set voltage, and takes a second value if the threshold voltage of the memory element is smaller than the set voltage,

wherein the first operation is performed if the verify signal takes the first value, and is not performed if the verify signal takes the second value, and

wherein the first operation and the second operation are terminated and the verify operation is finished when the verify signal changes from the first value to the second value.

12. A driving method according to claim 10, wherein the first period is 1μsec or shorter.

13. A driving method according to claim 11, wherein the first period is 1μ sec or shorter.

14. A driving method according to claim 1, wherein the memory element stores multi-state data.

15. A driving method according to claim 2, wherein the memory element stores

multi-state data.

16. A driving method according to claim 4, wherein the memory element stores multi-state data.

17. A driving method according to claim 8, wherein the memory element stores multi-state data.

18. A driving method according to claim 9, wherein the memory element stores multi-state data.

19. A driving method according to claim 10, wherein the memory element stores multi-state data.

20. A driving method according to claim 11, wherein the memory element stores multi-state data.

21. A nonvolatile memory driving method according to claim 8, wherein the first operation is performed by one of charge injection and charge discharge using a tunnel current.

22. A nonvolatile memory driving method according to claim 9, wherein the first operation is performed by one of charge injection and charge discharge using a tunnel current.

23. A nonvolatile memory driving method according to claim 10, wherein the first operation is performed by one of charge injection and charge discharge using a tunnel current.

24. A nonvolatile memory driving method according to claim 11, wherein the first operation is performed by one of charge injection and charge discharge using a tunnel current.

25. A nonvolatile memory driving method according to claim 8, wherein a potential difference exists between a source and a drain of the memory element during the second period.

26. A nonvolatile memory driving method according to claim 9, wherein a potential difference exists between a source and a drain of the memory element during the second period.

27. A nonvolatile memory driving method according to claim 10, wherein a potential difference exists between a source and a drain of the memory element during the second period.

28. A nonvolatile memory driving method according to claim 11, wherein a potential difference exists between a source and a drain of the memory element during the second period.

29. A nonvolatile memory driving method according to claim 8, wherein the first operation is performed by charge injection using a hot electron.

30. A nonvolatile memory driving method according to claim 9, wherein the first operation is performed by charge injection using a hot electron.

31. A nonvolatile memory driving method according to claim 10, wherein the first operation is performed by charge injection using a hot electron.

32. A nonvolatile memory driving method according to claim 11, wherein the first operation is performed by charge injection using a hot electron.

33. A nonvolatile memory that performs a verify operation, comprising:

a means for simultaneously performing a first operation for changing a threshold voltage of a memory element and a second operation for judging the threshold voltage of the memory element.

34. A nonvolatile memory that performs a verify operation, comprising:

a means for simultaneously performing a first operation for changing a threshold voltage of a memory element by one of charge injection and charge discharge using a tunnel current and a second operation for judging the threshold voltage of the memory element.

35. A nonvolatile memory according to claim 34, wherein a potential difference exists between a source and a drain of the memory element during the second operation.

36. A nonvolatile memory that performs a verify operation, comprising:

a means for simultaneously performing a first operation for changing a threshold voltage of a memory element by charge injection using a hot electron and a second operation for judging the threshold voltage of the memory element.

37. A nonvolatile memory according to claim 33, further comprising:

a means for terminating the first operation and the second operation and finishing the verify operation at a timing when the threshold voltage of the memory element judged by the second operation becomes a set voltage.

38. A nonvolatile memory according to claim 34, further comprising:

a means for terminating the first operation and the second operation and finishing the verify operation at a timing when the threshold voltage of the memory element judged by the second operation becomes a set voltage.

39. A nonvolatile memory according to claim 36, further comprising:

a means for terminating the first operation and the second operation and finishing the verify operation at a timing when the threshold voltage of the memory element judged by the second operation becomes a set voltage.

40. A nonvolatile memory that performs a verify operation for setting a

threshold voltage of a memory element at a set voltage or higher, the nonvolatile memory comprising:

a means for simultaneously performing a first operation for increasing the threshold voltage of the memory element and a second operation for judging a relation between the threshold voltage of the memory element and the set voltage;

a means for, during the second operation, generating a verify signal that takes a first value if the threshold voltage of the memory element is smaller than the set voltage and takes a second value if the threshold voltage of the memory element is larger than the set voltage;

a means for performing the first operation if the verify signal takes the first value, and not performing the first operation if the verify signal takes the second value; and

a means for terminating the first operation and the second operation and finishing the verify operation when the verify signal changes from the first value to the second value.

41. A nonvolatile memory that performs a verify operation for setting a threshold voltage of a memory element at a set voltage or lower, the nonvolatile memory comprising:

a means for simultaneously performing a first operation for decreasing the threshold voltage of the memory element and a second operation for judging a relation between the threshold voltage of the memory element and the set voltage;

a means for, during the second operation, generating a verify signal that takes a first value if the threshold voltage of the memory element is larger than the set

voltage and takes a second value if the threshold voltage of the memory element is smaller than the set voltage;

a means for performing the first operation if the verify signal takes the first value, and not performing the first operation if the verify signal takes the second value; and

a means for terminating the first operation and the second operation and finishing the verify operation when the verify signal changes from the first value to the second value.

42. A nonvolatile memory that performs a verify operation for setting a threshold voltage of a memory element at a set voltage or higher, the nonvolatile memory comprising:

a means for simultaneously performing a first operation for increasing the threshold voltage of the memory element and a second operation for judging a relation between the threshold voltage of the memory element and the set voltage;

a means for generating a verify signal that takes a first value during a first period;

a means for, during a second period, generating a verify signal that takes the first value if the threshold voltage of the memory element is smaller than the set voltage, and takes a second value if the threshold voltage of the memory element is larger than the set voltage;

a means for performing the first operation if the verify signal takes the first value, and not performing the first operation if the verify signal takes the second value; and

a means for terminating the first operation and the second operation and finishing the verify operation when the verify signal changes from the first value to the second value.

43. A nonvolatile memory that performs a verify operation for setting a threshold voltage of a memory element at a set voltage or lower, the nonvolatile memory comprising:

a means for simultaneously performing a first operation for decreasing the threshold voltage of the memory element and a second operation for judging a relation between the threshold voltage of the memory element and the set voltage;

a means for generating a verify signal that takes a first value during a first period;

a means for, during a second period, generating a verify signal that takes the first value if the threshold voltage of the memory element is larger than the set voltage, and takes a second value if the threshold voltage of the memory element is smaller than the set voltage;

a means for performing the first operation if the verify signal takes the first value, and not performing the first operation if the verify signal takes the second value; and

a means for terminating the first operation and the second operation and finishing the verify operation when the verify signal changes from the first value to the second value.

44. A nonvolatile memory according to claim 42, wherein the first period is 1

μsec or shorter.

45. A nonvolatile memory according to claim 43, wherein the first period is 1 μsec or shorter.

46. A nonvolatile memory according to claim 33, wherein the memory element stores multi-state data.

47. A nonvolatile memory according to claim 34, wherein the memory element stores multi-state data.

48. A nonvolatile memory according to claim 36, wherein the memory element stores multi-state data.

49. A nonvolatile memory according to claim 40, wherein the memory element stores multi-state data.

50. A nonvolatile memory according to claim 41, wherein the memory element stores multi-state data.

51. A nonvolatile memory according to claim 42, wherein the memory element stores multi-state data.

52. A nonvolatile memory according to claim 43, wherein the memory element

stores multi-state data.

53. A nonvolatile memory according to claim 40, wherein the first operation is performed by one of charge injection and charge discharge using a tunnel current.

54. A nonvolatile memory according to claim 41, wherein the first operation is performed by one of charge injection and charge discharge using a tunnel current.

55. A nonvolatile memory according to claim 42, wherein the first operation is performed by one of charge injection and charge discharge using a tunnel current.

56. A nonvolatile memory according to claim 43, wherein the first operation is performed by one of charge injection and charge discharge using a tunnel current.

57. A nonvolatile memory according to claim 40. wherein during the second operation, a potential difference exists between a source and a drain of the memory element.

58. A nonvolatile memory according to claim 41, wherein during the second operation, a potential difference exists between a source and a drain of the memory element.

59. A nonvolatile memory according to claim 42, wherein during the second operation, a potential difference exists between a source and a drain of the memory element.

60. A nonvolatile memory according to claim 43, wherein during the second

operation, a potential difference exists between a source and a drain of the memory element.

61. A nonvolatile memory according to claim 40, wherein the first operation is performed by charge injection using a hot electron.

62. A nonvolatile memory according to claim 41, wherein the first operation is performed by charge injection using a hot electron.

63. A nonvolatile memory according to claim 42, wherein the first operation is performed by charge injection using a hot electron.

64. A nonvolatile memory according to claim 43, wherein the first operation is performed by charge injection using a hot electron.

65. A nonvolatile memory according to claim 33, wherein the memory element is an n-channel type memory element.

66. A nonvolatile memory according to claim 34, wherein the memory element is an n-channel type memory element.

67. A nonvolatile memory according to claim 36, wherein the memory element is an n-channel type memory element.

68. A nonvolatile memory according to claim 40, wherein the memory element

is an n-channel type memory element.

69. A nonvolatile memory according to claim 41, wherein the memory element is an n-channel type memory element.

70. A nonvolatile memory according to claim 42, wherein the memory element is an n-channel type memory element.

71. A nonvolatile memory according to claim 43, wherein the memory element is an n-channel type memory element.

72. A nonvolatile memory according to claim 33, wherein the memory element is a p-channel type memory element.

73. A nonvolatile memory according to claim 34, wherein the memory element is a p-channel type memory element.

74. A nonvolatile memory according to claim 36, wherein the memory element is a p-channel type memory element.

75. A nonvolatile memory according to claim 40, wherein the memory element is a p-channel type memory element.

76. A nonvolatile memory according to claim 41, wherein the memory element

is a p-channel type memory element.

77. A nonvolatile memory according to claim 42, wherein the memory element is a p-channel type memory element.

78. A nonvolatile memory according to claim 43, wherein the memory element is a p-channel type memory element.

79. A nonvolatile memory according to one of claim 33, wherein the nonvolatile memory is a NOR type nonvolatile memory.

80. A nonvolatile memory according to one of claim 34, wherein the nonvolatile memory is a NOR type nonvolatile memory.

81. A nonvolatile memory according to one of claim 36, wherein the nonvolatile memory is a NOR type nonvolatile memory.

82. A nonvolatile memory according to one of claim 40, wherein the nonvolatile memory is a NOR type nonvolatile memory.

83. A nonvolatile memory according to one of claim 41, wherein the nonvolatile memory is a NOR type nonvolatile memory.

84. A nonvolatile memory according to one of claim 42, wherein the nonvolatile

memory is a NOR type nonvolatile memory.

85. A nonvolatile memory according to one of claim 43, wherein the nonvolatile memory is a NOR type nonvolatile memory.

86. A nonvolatile memory according to claim 33, wherein the nonvolatile memory is a NAND type nonvolatile memory.

87. A nonvolatile memory according to claim 34, wherein the nonvolatile memory is a NAND type nonvolatile memory.

88. A nonvolatile memory according to claim 36, wherein the nonvolatile memory is a NAND type nonvolatile memory.

89. A nonvolatile memory according to claim 40, wherein the nonvolatile memory is a NAND type nonvolatile memory.

90. A nonvolatile memory according to claim 41, wherein the nonvolatile memory is a NAND type nonvolatile memory.

91. A nonvolatile memory according to claim 42, wherein the nonvolatile memory is a NAND type nonvolatile memory.

92. A nonvolatile memory according to claim 43, wherein the nonvolatile

memory is a NAND type nonvolatile memory.

93. A semiconductor device that uses a nonvolatile memory according to claim 33 as a recording medium.

94. A semiconductor device that uses a nonvolatile memory according to claim 34 as a recording medium.

95. A semiconductor device that uses a nonvolatile memory according to claim 36 as a recording medium.

96. A semiconductor device that uses a nonvolatile memory according to claim 40 as a recording medium.

97. A semiconductor device that uses a nonvolatile memory according to claim 41 as a recording medium.

98. A semiconductor device that uses a nonvolatile memory according to claim 42 as a recording medium.

99. A semiconductor device that uses a nonvolatile memory according to claim 43 as a recording medium.

100. A semiconductor device according to claim 93, wherein the semiconductor

device is a microprocessor.

101. A semiconductor device according to claim 94, wherein the semiconductor device is a microprocessor.

102. A semiconductor device according to claim 95, wherein the semiconductor device is a microprocessor.

103. A semiconductor device according to claim 96, wherein the semiconductor device is a microprocessor.

104. A semiconductor device according to claim 97, wherein the semiconductor device is a microprocessor.

105. A semiconductor device according to claim 98, wherein the semiconductor device is a microprocessor.

106. A semiconductor device according to claim 99, wherein the semiconductor device is a microprocessor.

107. A semiconductor device according to claim 93, wherein the semiconductor device is one of a display, a video camera, a head mount type display, a DVD player, a goggle type display, a personal computer, a mobile telephone, and a car audio equipment.

108. A semiconductor device according to claim 94, wherein the semiconductor device is one of a display, a video camera, a head mount type display, a DVD player, a goggle type display, a personal computer, a mobile telephone, and a car audio equipment.

109. A semiconductor device according to claim 95, wherein the semiconductor device is one of a display, a video camera, a head mount type display, a DVD player, a goggle type display, a personal computer, a mobile telephone, and a car audio equipment.

110. A semiconductor device according to claim 96, wherein the semiconductor device is one of a display, a video camera, a head mount type display, a DVD player, a goggle type display, a personal computer, a mobile telephone, and a car audio equipment.

111. A semiconductor device according to claim 97, wherein the semiconductor device is one of a display, a video camera, a head mount type display, a DVD player, a goggle type display, a personal computer, a mobile telephone, and a car audio equipment.

112. A semiconductor device according to claim 98, wherein the semiconductor device is one of a display, a video camera, a head mount type display, a DVD player, a goggle type display, a personal computer, a mobile telephone, and a car audio equipment.

113. A semiconductor device according to claim 99, wherein the semiconductor device is one of a display, a video camera, a head mount type display, a DVD player, a goggle type display, a personal computer, a mobile telephone, and a car audio equipment.